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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,211	02/14/2002	Richard J. Nathan	M-12562 US	3098
34036	7590	02/27/2004	EXAMINER	
SILICON VALLEY PATENT GROUP LLP 2350 MISSION COLLEGE BOULEVARD SUITE 360 SANTA CLARA, CA 95054			ZARNEKE, DAVID A	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/077,211

Applicant(s)

NATHAN ET AL.

Examiner

David A. Zarneke

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-29 is/are allowed.
- 6) ☒ Claim(s) 30-49 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments filed 11/19/03, with respect to claims 1-29 have been fully considered and are persuasive. The rejection of 7/1/03 has been withdrawn. The amendment to the claims, which conforms with the language discussed in the interview summary of 11/3/03, puts them in condition of allowance.

Applicant's arguments with respect to new claims 31-49 have been considered but are moot in view of the new ground(s) of rejection.

It is argued that the limitation in the independent claims 30 and 48 reciting "each trace ends on the top surface of said substrate in a conductive land or pad, and is integrally formed on the substrate" is not taught by Mahulikar. Specifically, that the use of the phrase "trace" excludes the bond wires used in Mahulikar.

The examiner agrees with this argument, but submits a new rejection of the claims below.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Drye et al., US Patent 4,722,914.

Drye teaches a structure (figures 4A-4D) comprising:

- a substrate formed of a heat deformable material (41);
- at least one semiconductor die (42) embedded in said substrate such that the top surfaces of said at least one semiconductor die and the top surface of said substrate are in substantially the same plane (figures);
- a plurality of bonding pads formed on the top surfaces of said at least one die (44); and
- a plurality of traces of conductive material (46 & 47) formed over the top surfaces of said at least one die and the top surface of said substrate, each trace beginning in electrical contact with a corresponding bonding pad on said at least one die, and each trace ending on the top surface of said substrate in a conductive land or pad and being integrally formed on said substrate. each trace electrically connecting said corresponding bonding pad on the top surfaces of said at least one die with said corresponding conductive land or pad on the top surface of said substrate (figures).

Claims 48 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Drye et al., US Patent 4,722,914.

Drye teaches a structure comprising:

- a substrate formed of a heat deformable material (41);
- a semiconductor die (42) embedded in said substrate such that the top surface of said semiconductor die and the top surface of said substrate are both exposed;
- a plurality of bonding pads formed on the top surface of said semiconductor die (44); and

a plurality of traces of conductive material (46 & 47) formed over the top surface of said substrate, each trace ending on said top surface of said semiconductor die at one of said plurality of bonding pads and each trace starting on said top surface of said substrate as a conductive land and integrally formed thereon (figures).

Regarding claim 49, Drye teaches the top surface of said semiconductor die and the top surface of said substrate are substantially coplanar (figures).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drye et al., US Patent 4,722,914, as applied to claim 30 above, and further in view of Mahulikar, US Patent 6,528,351.

Regarding claims 31-33, Drye fails to teach including a plurality of conductive balls, each ball being formed on a corresponding one of the conductive lands or pads on the top of said substrate, and conductive balls allowing said structure to be electrically connected to electrical contacts on an additional substrate.

Mahulikar teaches a BGA package comprising:

- a substrate (62) formed of a heat deformable material, such as a metal, polymer or ceramic (6, 50+);

- at least one semiconductor die (54) embedded in said substrate such that the top surface(s) of said at least one semiconductor die and the top surface of said substrate are in substantially the same plane;

- a plurality of bonding pads formed on the top surface(s) of said at least one die;

- and a plurality of conductive paths (66) formed over the top surface(s) of said at least one die and the top surface of said substrate, each conductive path ending on the top surface of said substrate in a conductive land or pad and beginning in

electrical contact, using a bond wire (58), with a corresponding bonding pad on said at least one die thereby to connect said corresponding bonding pad on the top surface(s) of said at least one die with a corresponding conductive land or pad on the top surface of said substrate (Figure 9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the invention of Mahulikar in the invention of Drye because Mahulikar teaches acceptable alternative equivalent methods of using the embedded die structure.

Mahulikar further teaches the use of solder balls (70) to attach the lands of the package to contacts on a PCB (92), the PCB inherently having conductive traces connected to said electrical contacts thereby to allow electrical signals to be sent from said at least one die to circuitry external to said at least one die and to also allow electrical signals to be sent from circuitry external to said at least one die to said at least one die.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claims 34 and 35, Mahulikar teaches depositing a potting compound (60) over the die that can be made of epoxy (6, 16+).

As to claim 36, Mahulikar teaches the potting compound as covering some of the substrate surface (Figure 9). The term "covers" does not inherently imply complete coverage, only that some of the surface is covered.

Regarding claim 37, Mahulikar teaches a substrate having bond pads on its bottom side and vias through the substrate connecting bond pads on the top surface with bond pads on the top side (Figures 15-18).

Claims 38-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drye et al., US Patent 4,722,914, in view of Mahulikar et al., US Patent 5,629,835, as applied to claim 30 above, and further in view of Hamburgers et al., US Patent 5,776,800.

Regarding claim 38, Mahulikar fails to teach forming a conductive plane over the top of the die, wherein the plane is electrically insulated from the bonding pads of the die.

Hamburger teaches a metallic stress relieving insert (43) formed over the top of the die and electrically insulated from the bonding pads of the die (figure 10).

It would have been obvious to one of ordinary skill in the art to use the metallic stress relieving insert of Hamburgers in the invention of Mahulikar because the metallic stress relieving insert relieves thermal and mechanical stresses.

With respect to claim 39, Mahulikar fails to teach forming a conductive plane over the top of the die in a region interior to the bonding pads of the die.

Hamburger teaches a metallic stress relieving insert (43) formed over the top of the die and interior to the bonding pads of the die (figure 10).



It would have been obvious to one of ordinary skill in the art to use the metallic stress relieving insert of Hamburgren in the invention of Mahulikar because the metallic stress relieving insert relieves thermal and mechanical stresses without taking up much space.

As to claims 40, 41 and 47, Hamburgren teaches electrically connecting the plane to bumps on the chip to act as a chip capacitor (figure 11).

It would have been obvious to one of ordinary skill in the art to use the chip capacitor of Hamburgren in the invention of Mahulikar because Hamburgren teaches that the chip capacitor stabilizes the power supply (5, 55+).

Regarding claim 42, while Hamburgren fails to teach forming an isolative protective coating over the plane, it is conventionally known to one of ordinary skill in the art to bury the insert of Hamburgren because the exposed surface of the insert would then be protected from the environment.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

With respect to claims 43 and 44, the protective coating having openings therein and conductive materials deposited into these openings so as to provide electrical connection and attachment to an external heat sink.

The forming of openings having conductive materials therein to provide connection to the plane and to provide attachment to an external heat sink is conventionally known in the art.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

As to claims 45-46, the use of a bottom conductive plane that is electrically connected to a source of potential such as ground and power.

The use of a bottom plane that is electrically connected a ground or power supply is conventionally known in the art.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

### ***Allowable Subject Matter***

Claims 1-29 have been allowed over the prior art.

The following is a statement of reasons for the indication of allowable subject matter: The concept of "embedding" the die in the heat deformable material so that the top of the die is coplanar with the top of the substrate is novel.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

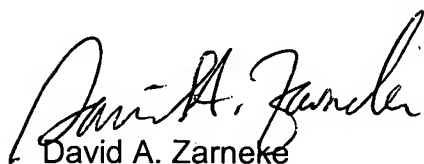
Fillion et al., US Patent 5,353,498, McMahon, US Patent 5,375,041, Cole, Jr. et al., US Patent 5,745,984, Wojnarowski, US Patent 5,949,133, Chiou et al., US Patent 6,309,912, and Nishiguchi, US Patent 5,188,984 are all cited as teaching the state of the art.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David A. Zarneke  
Primary Examiner  
February 4, 2004